CLEAN VERSION OF ALL PENDING CLAIMS:

1. (Amended five times) A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material, said alignment component consisting of a single material;

depositing a metal layer directly on a top and sides of the alignment component and directly on a region of the substrate adjacent to the alignment component, wherein previous to said depositing the region of the substrate adjacent to the alignment component has not been doped differently than a region of the substrate covered by the alignment component;

reacting the metal layer with the semiconductor material of the substrate to form two silicide regions, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate;

removing the alignment component; and

replacing the removed alignment component with a conductive gate.

2. The method of claim 1 wherein the alignment component is non-conductive.

3. (Amended once) The method of claim 2 wherein the alignment component includes a material selected from the group consisting of a silicon oxide and silicon nitride.

4. (Amended once) The method of claim 1 wherein the alignment component includes a material which is non-reactive with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

5. The method of claim 1 wherein the alignment component has a thickness of between 1000Å and 2500Å.

6. The method of claim 1 wherein the alignment component is less than 0.10 microns wide.

7. (Amended once) The method of claim 1 wherein the metal layer includes material selected from the group consisting of tungsten, cobalt and titanium.

8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å thick.

9. (Amended once) The method of claim 1 wherein the silicide regions have lower surfaces located lower than a lower surface of the alignment component.

10. (Amended four times) The method of claim 1 wherein said removing the alignment component includes:

depositing a layer over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed; and

etching the alignment component at least until the substrate is exposed to leave an opening between the inner surfaces of the silicide regions to allow for formation of the gate.

11. (Amended twice) The method of claim 10 further comprising exposing the upper portions of the inner surfaces after said etching of the alignment component.

12. (Amended once) The method of claim 10 wherein the alignment component and the layer are of different materials, one being of silicon oxide and the other being of silicon nitride.

13. (Amended once) The method of claim 1 wherein said replacing with the conductive gate includes:

depositing a gate dielectric layer; and

forming a gate electrode on the gate dielectric layer.

14. The method of claim 13 wherein the gate dielectric layer is less than 10Å thick.

15. (Amended once) The method of claim 13 wherein the gate electrode includes a metal.

16. The method of claim 1, further comprising:

forming doped regions which extend from the silicide regions in underneath the gate.

17. The method of claim 13 wherein the gate dielectric layer has a dielectric constant of at least 100.

18. (Amended once) The method of claim 13 wherein the gate dielectric layer includes a material selected from the group consisting of strontium titanate, and barium strontium titanate.

19. (Amended once) The method of claim 17 wherein the gate electrode includes a material selected from the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.

28. (Amended once) The method of claim 1, wherein the metal layer includes nickel and the silicide regions extend partially below the alignment component.

29. (Amended once) The method of claim 1, wherein the alignment component includes a material that does not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

30. (Amended once) The method of claim 29, further comprising removing a portion of the metal layer above the alignment component after the metal layer is reacted with the semiconductor material of the substrate.

31. (Amended once) The method of claim 1, wherein the gate dielectric layer is made of silicon oxide and has a thickness of less than 10 Å.

32. (Amended once) The method of claim 1, wherein removing the alignment component comprises:

depositing a layer of a different material than the alignment component over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed; and

etching the alignment component at least until the substrate and the upper portions of each inner surface of the silicide regions are exposed.

REMARKS

Claims 1-12, 16, 29, 30 and 32 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 6,063,677 ("Rodder") in view of U.S. patent no. 5,937,300 ("Sekine") and U.S. patent no. 6,051,473 ("Ishida"). Claims 13-15 and 31 have been rejected under 35 USC 103(a) as being unpatentable over Rodder, Sekine, and Ishida, and further in view of U.S. patent 6,054,355 ("Inumiya"). Claims 17-19 have been rejected under 35 USC 103(a) as being unpatentable over Rodder, Sekine, Ishida, and Inumiya and further in view of U.S. patent 6,051,865 ("Gardner"). Claim 28 has been rejected under 35 USC 103(a) as being unpatentable over Rodder, Sekine, and